What is claimed is:

1. A method of manufacturing a flash memory cell, comprising the steps of:

forming an isolation film having a projection that is projected higher than the surface of a semiconductor substrate in an isolation region of the semiconductor substrate;

forming a first tunnel oxide film on the semiconductor substrate;

depositing a material film for a first floating gate on the semiconductor substrate on which the first tunnel oxide film is formed;

patterning the material film for the first floating gate;

sequentially forming a second tunnel oxide film and a material film for a second floating gate over the semiconductor substrate on which the material film for the patterned first floating gate is formed along the step;

isolating the material film for the first floating gate by means of the projection while removing the second tunnel oxide film on the material film for the first floating gate and the material film for the second floating gate by means of chemical mechanical polishing;

forming a material film for a control gate and a hard mask layer on the resulting surface; and

patterning the hard mask layer, the material film for the control gate, the material film for the second floating gate, the second tunnel oxide film, the material film for the first floating gate and the first tunnel oxide film, using a mask defining a gate pattern.

2. The method as claimed in claim 1, further comprising the step of etching the projection of the isolation film formed between the material film for the first floating gates, before the step of forming the material film for the control gate and the hard mask layer.

3. The method as claimed in claim 1, wherein the step of forming the isolation film having the projection comprising the sub steps of:

forming a pad oxide film and a pad nitride film on the semiconductor substrate;

etching the pad nitride film, the pad oxide film and the semiconductor substrate using the mask defining the isolation region, thus forming a trench;

forming an oxide film along the sidewall of the trench;

forming a trench type isolation film that buries the trench up to the top surface of the patterned pad nitride film;

removing the pad nitride film; and

removing the pad oxide film.

4. The method as claimed in claim 1, wherein the first tunnel oxide film is formed by means of a wet oxidization mode

5. The method as claimed in claim 1, wherein the second tunnel oxide film is formed using a high-temperature oxide film.

6. The method as claimed in claim 1, wherein the second tunnel

oxide film is formed in thickness of 50 ~ 100 Å.

7. The method as claimed in claim 1, wherein the material film for the first floating gate is a polysilicon film.

8. The method as claimed in claim 1, wherein the material film for the second floating gate is a silicon nitride film.

9. The method as claimed in claim 1, wherein the material film for the second floating gate is formed in thickness of 100 ~ 1000 Å.

10. The method as claimed in claim 1, wherein the dielectric film is formed by sequentially stacking a silicon oxide film, a silicon nitride film and a silicon oxide film.

11. A flash memory cell, comprising:

a first tunnel oxide film formed at a given region of a semiconductor substrate;

a first floating gate formed on the first tunnel oxide film;

a second tunnel oxide film formed over the semiconductor substrate and along one sidewall of the first floating gate;

a second floating gate isolated from the first floating gate while contacting the second tunnel oxide film;

a dielectric film formed on the first floating gate and the second floating

gate;

a control gate formed on the dielectric film;

a first junction region formed in the semiconductor substrate below one side of the second tunnel oxide film; and

a second junction region formed in the semiconductor substrate below one side of the first tunnel oxide film.

12. The flash memory cell as claimed in claim 11, wherein data of 2-bit is stored at 1 (one) cell, by injecting electrons into the first floating gate and the second floating gate and discharging electrons injected into the first floating gate and the second floating gate depending on a voltage applied to the control gate, the first junction region and the second junction region.

13. The flash memory cell as claimed in claim 11, wherein data of 3-bit is stored at 1(one) cell by storing data of 1 bit at the second floating gate and storing data of 2-bit at the first floating gate, by injecting electrons into the first floating gate and the second floating gate and discharging electrons injected into the first floating gate and the second floating gate, depending on a voltage applied to the control gate, the first junction region and the second junction region.

14. The flash memory cell as claimed in claim 11, wherein the second tunnel oxide film is formed using a high-temperature oxide film.

15. The flash memory cell as claimed in claim 11, wherein the second tunnel oxide film has a thickness of 50 ~ 100 Å.

16. The flash memory cell as claimed in claim 11, wherein the first floating gate is formed using a polysilicon film and the second floating gate is formed using a silicon nitride film.

17. The flash memory cell as claimed in claim 11, wherein the first floating gate has a thickness of 500 ~ 2000 Å.

18. The flash memory cell as claimed in claim 11, wherein the second floating gate has a thickness of 100 ~ 1000 Å.

19. A programming method of a flash memory cell for storing data at the flash memory cell claimed in claim 11, being characterized in that:

if electrons are to be injected into the first floating gate, a programming operation is performed by applying a programming voltage to the control gate, connecting the first junction region and the ground terminal and applying a voltage lower than the programming voltage but higher than the ground voltage to the second junction region, and

if the electrons are to be injected into the second floating gate, the programming operation is performed by applying a programming voltage to the control gate, applying a voltage lower than the programming voltage but higher than the ground voltage to the first junction region and connecting the

second junction region and the ground terminal,

wherein the programming operations are independently performed for the first floating gate and the second floating gate.

20. The programming method as claimed in claim 19, wherein the programming voltage is 7V ~ 9V, and the voltage lower than the programming voltage but higher than the ground voltage is 4V ~ 5V.

21. An erasing method of a flash memory cell for erasing data stored at the flash memory cell claimed in claim 11, being characterized in that:

if electrons injected into the first floating gate are to be discharged, an erasing operation is performed by applying an erasing voltage to the control gate, and applying a voltage higher than the ground voltage to the second junction region with the first junction region floated, and

if electrons injected into the second floating gate are to be discharged, the erasing operation is performed by applying the erasing voltage to the control gate, and applying a voltage higher than the ground voltage to the first junction region with the second junction region floated,

wherein the erasing operations are independently performed for the first floating gate and the second floating gate.

22. The erasing method as claimed in claim 21, wherein the erasing voltage is -8V ~ -9V, and the voltage higher than the ground voltage is 4V ~

5V.

23. An erasing method of a flash memory cell for erasing data stored at the flash memory cell claimed in claim 11, being characterized in that:

an erasing operation is performed by simultaneously discharging electrons injected into the first floating gate and the second floating gate, by applying an erasing voltage to the control gate and a voltage higher than the ground voltage to the semiconductor substrate, with the first junction region and the second junction region floated.

24. The erasing method as claimed in claim 23, wherein the erasing voltage is -8V ~ -9V, and the voltage higher than the ground voltage is 8V ~ 9V.

25. A reading method of a flash memory cell for reading data stored at the flash memory cell claimed in claim 11, being characterized in that:

a reading operation is performed by applying a reading voltage to the control gate, connecting the first junction region to the ground terminal, applying a voltage lower than the reading voltage but higher than the ground voltage to the second junction region and then sensing cell current flowing into the second junction region, or by applying the reading voltage to the control gate, connecting the second junction region to the ground terminal, applying a

voltage lower than the reading voltage but higher the ground voltage to the first junction region, and then sensing cell current flowing into the first junction region.

26. The reading method as claimed in claim 24, wherein the reading voltage is 4V ~ 5V, and the voltage lower than the reading voltage but higher than the ground voltage is 0.8V ~ 1V.